IN THE CLAIMS:

1-20 (Cancelled)

21. (Original) A semiconductor device, comprising:
a first die attach paddle made of an electrically conductive material;
a second die attach paddle made of an electrically conductive material; and
at least one semiconductor die having a bottom surface attached to said first and second die attach paddles;
wherein the first and second die attach paddles are electrically separated from each other.

22. (Withdrawn) The semiconductor device of claim 21, wherein:
the semiconductor device comprises one semiconductor die;
the bottom surface of said one semiconductor die has a first part and a second part;
the first part of the bottom surface is attached to said first die attach paddle; and
the second part of the bottom surface is attached to said first die attach paddle.

23. (Withdrawn) The semiconductor device of claim 22, wherein the first and second parts of the bottom surface are electrically connected to the respective die attach paddles.

24. (Withdrawn) The semiconductor device of claim 23, wherein:
the semiconductor die carries a first circuitry and a second circuitry;
the first part of the bottom surface provides a ground contact of the first circuitry; and
the second part of the bottom surface provides a ground contact of the second circuitry.

25. (Withdrawn) The semiconductor device of claim 24, wherein the first circuitry is an analog circuitry for processing analog signals, and the second circuitry is a digital circuitry for processing digital signals.

26. (Withdrawn) The semiconductor device of claim 24, wherein the first and second die attach paddles are shaped corresponding to the shapes of the first and second parts of the bottom surface, respectively.

27. (Withdrawn) The semiconductor device of claim 23, wherein the first and second die attach paddles are exposed on the bottom surface of the semiconductor device package.

28. (Original) The semiconductor device of claim 21, wherein:
the semiconductor device comprises two semiconductor dies;
said bottom surface has a first part relating to the first semiconductor die and a second part relating to the second semiconductor die;
the first part of the bottom surface is attached to said first die attach paddle; and
the second part of the bottom surface is attached to said first die attach paddle.

29. (Original) The semiconductor device of claim 28, wherein the first and second parts of the bottom surface are electrically connected to the respective die attach paddles.

30. (Original) The semiconductor device of claim 29, wherein:
the first part of the bottom surface provides a ground contact of the first semiconductor die; and
the second part of the bottom surface provides a ground contact of the second semiconductor die.

31. (Original) The semiconductor device of claim 30, wherein the first semiconductor die is arranged for processing analog signals, and the second semiconductor die is arranged for processing digital signals.

32. (Original) The semiconductor device of claim 30, wherein the first and second die attach paddles are shaped corresponding to the shapes of the first and second parts of the bottom surface, respectively.

33. (Original) The semiconductor device of claim 29, wherein the first and second die attach paddles are exposed on the bottom surface of the semiconductor device package.

34. (Original) The semiconductor device of claim 21, wherein the first and second die attach paddles are connected to provide ground contacts for analog and digital signals, respectively.

35. (Original) The semiconductor device of claim 21, wherein the at least one semiconductor die carries a first circuitry and a second circuitry;

the bottom surface provides a first contact relating to the first circuitry and a second contact relating to the second circuitry;

the first and second die attach paddles are attached to the first and second contacts, respectively; and

the first and second die attach paddles correspond in shape to the respective first and second contacts.

36. (Original) The semiconductor device of claim 21, wherein said at least one semiconductor die comprises integrated circuits for processing analog and digital signals having frequencies of greater than 5 GHz.

37. (Original) The semiconductor device of claim 21, further comprising a plurality of leads for, when electrically connected to the at least one semiconductor die, providing electrical contacts to the at least one semiconductor die, said plurality of leads being held together thereby forming a lead frame.

38. (Original) The semiconductor device of claim 37, wherein said first and second die attach paddles are fixed to said lead frame.

39. (Original) The semiconductor device of claim 37, wherein at least one of said first and second die attach paddles is fixed to a paddle lead on a corner of said lead frame.

40. (Original) The semiconductor device of claim 39, wherein said at least one die attach paddle is further fixed to a second paddle lead on another corner of said lead frame.

41. (Original) The semiconductor device of claim 39, wherein said at least one die attach paddle is further fixed to at least one of said plurality of leads.

42. (Original) The semiconductor device of claim 37, wherein at least one of said first and second die attach paddles has a three point connection to said lead frame.

43. (Original) The semiconductor device of claim 37, wherein at least one of said first and second die attach paddles is fixed to said lead frame at multiple connection points, the number of connection points being greater than four.

44. (Original) The semiconductor device of claim 21, further comprising a plurality of leads for, when electrically connected to the at least one semiconductor die, providing electrical contacts to the at least one semiconductor die,

wherein at least one of said first and second die attach paddles is fixed to one of said plurality of leads.

45. (Original) The semiconductor device of claim 44, wherein said plurality of leads are arranged in the package to substantially form a rectangle, and said one of said plurality of leads is located near the center of one side of said rectangle.

46. (Original) The semiconductor device of claim 44, wherein:

said at least one of said first and second die attach paddles is further fixed to another one of said plurality of leads;

said another one of said plurality of leads is located adjacent to said one of said plurality of leads; and

said one and said another one of said plurality of leads form a multiple common lead.

47. (Original) The semiconductor device of claim 21, wherein the first and second die attach paddles each have a size of about half of the area of the bottom surface of the at least one semiconductor die.

48. (Original) The semiconductor device of claim 47, wherein the first and second die attach paddles each have a substantially rectangular shape.

49. (Original) The semiconductor device of claim 21, further comprising a plurality of leads for, when electrically connected to the at least one semiconductor die, providing electrical contacts to the at least one semiconductor die,

wherein the first and second die attach paddles are electrically separated from each other by providing a spatial distance between the first and the second die attach paddles, and said spatial distance is greater than the width of one of said plurality of leads.

50. (Original) The semiconductor device of claim 21, further comprising a plurality of leads for, when electrically connected to the at least one semiconductor die, providing electrical contacts to the at least one semiconductor die,

wherein the first and second die attach paddles are electrically separated from each other by providing a spatial distance between the first and the second die attach paddles, and said spatial distance is substantially equal to the distance of two adjacent leads of said plurality.

51-52 (Cancelled)